UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,154	08/26/2003	Gerald George Pechanek	1380001	3684

27997 7590 01/24/2006

PRIEST & GOLDSTEIN PLLC
5015 SOUTHPARK DRIVE
SUITE 230
DURHAM, NC 27713-7736

EXAMINER	
PAN, DANIEL H	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 01/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,154	PECHANEK, GERALD GEORGE	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,12-16,29,30,34-36 and 42* is/are rejected.

7)☒ Claim(s) *10,11,16-24,27,28,31-33 and 37-41* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/03/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-42 are presented for examination.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1,12 are rejected under 35 U.S.C. 102(b) as being anticipated by Kitamura et al. (5,197,145).

3. As to claim 1, 12, Kitamura taught at least (see fig.4) :

a) providing a set of arithmetic/logic instructions (see instructions from I buffer 25 and executed by arithmetic controller 21 in col.5, lines 67-68, col.6, lines 1-18);

b) storing set of instructions in at least one memory (I buffer 25);

c) providing a set of instruction fetch instructions (see microprogram in storage 23) for programmably selecting instructions to be fetched from said at least one memory [Buffer 25];

d) providing an memory [storage control 23] for storage of said set of fetch instructions (see microinstructions);

e) generating instruction fetch instructions and their sequencing for programmably selecting AL instructions to be fetched from said at least one arithmetic memory [I Buffer 25] (see how the instructions were fetched from I Buffer 25 under the address control of microinstructions in col.59-68, col.6, lines 1-28),

f) storing the sequence of instruction fetch instructions [microinstructions] in the memory [23]; and

g) fetching and executing said sequence of instructions to generate addresses for fetching AL instructions from said at least one AL memory and executing the fetched AL instructions, whereby the function of said program is accomplished (see the fetching and execution of the instructions by the arithmetic controller 21 and instruction processing controller 22 in col.59-68, col.6, lines 1-28 under address control of microinstructions, see also how the hit or miss tags were operated for memory access in col.6, lines 29-46) .

4. As to the decoder in claim 12, Kitamura also included a decoder (see fig.5 40 decoder).

Kitamura did not explicitly show the logic instruction as claimed. However, Kitamura showed arithmetic operations (see col.6, lines 7-12) and also showed a central processing unit in the background art (col.1, lines 33-36). The examiner holds that a logic operation or logic instruction was most likely in Kitamura because a CPU without a logic unit would be unusual.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 1-9, 12,42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata et al. (5,430,851) in view Blackmon et al. (6,895,482) .

6. As to claim 1,12, 42, Hirata disclosed at least :

a) providing a set of arithmetic/logic instructions (see fig. 2a and fig.3);

b) storing set of instructions in at least one memory (see instruction cache in fig.2a and fig.3);

c) fetch unit for programmably selecting instructions to be fetched from said at least one memory (see instruction fetch unit in fig.2a and fig.3);

g) fetching and executing said sequence of instructions to generate addresses for fetching instructions (see ADD, SUB instructions in fig.2a and fig.3, see also col.5, lines 55-69, col.6, lines 1-7) from said at least one memory (instruction ache) and executing the fetched instructions (see ALU, adder, Multiplier , Barrel Shifter in fig.2a) , whereby the function of said program is accomplished (see also function units in col.9, lines 8-23) .

7. As to the decoder in claims 12,42, see fig.2a [decoder].

8. Hirata did not specifically show the storage of the fetch instructions as claimed. However, Blackmon disclosed a system including a storage of fetch instructions (see the storage of fetch commands). It would have been obvious to one of n ordinary skill in the art to use of Blackmon in Hirata for including the storage of fetch instructions as claimed because the use of Blackmon could provide Hirata the ability to read the a

predefined set of instructions ion a corresponding storage based on the respective fetch, thereby increasing the accessibility of the predefined set of instructions as required , and therefore minimizing the overall hardware overheads of the memory, and because Hirata did disclosed his fetch unit for fetching instructions for reading instructions by giving memory or a cache the address designated by program counter of disposing instructions into a determined local instruction register and of generating various address for instructing access (see col.5, lines 65-69, col.6, lines 1-3), which was a suggestion of the need for providing a fetch command to designate the program counter for purpose of reading or fetching the instruction from the respective instruction set memories in order to increase the accessibility of the fetched instructions , and for doing so, provided a motivation. Hirata is used as primary reference because it shows clearly the ADD, SUB, MUL instructions (see fig.2a). Blackmon is used to supplement the teaching of IF instructions or commands in a storage (see fig.9).

9. As to claim 2, Hirata also included add and subtract instructions (see fig.2a).

10. As to claim 3, Hirata also accessed memory multiple times (see the multiple instruction fetch in col.5, lines 55,56).

11. As to claims 4,6, Hirata also included selected set of parallel instructions (see parallel instruction stream in col.5, lines 58-64).

12. As to claim 5, see the single instruction stream in col.5, lines 57-60).

13. As to the if-then-else, for-do, call , return instruction structures in claim 7, examiner holds that theses structures have been known in the art. Since no specific

format is being reflected into the claim, it is assumed to be read on any known instruction structures.

14. As to claim 8, Hirata also identified selected instruction (see the program counter in col.5, lines 65-68, see also the directive tags in col.6, lines 19-61, see also Table 2, see multi-instruction issue in col.9, lines 45-49).

15. As to claim 9, see program counter in col.5, lines 65-68 for sequence of instructions .

16. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata et al. (5,430,851) in view Blackmon et al. (6,895,482) as applied to claim 12 above, and further in view of Kishida et al. (6.065,112).

17. As to claim 13, neither Hirata nor Blackmon specifically disclosed the opcode field specifying the number of sequential instruction fetch as claimed. However, Kishida disclosed a system including an instruction field for specifying number of sequential fetch instructions (see col.14, lines 22-37). It would have been obvious to one of ordinary skill in the art to use Kishida in Hirata for including the opcode field for specifying the number of sequential fetch instructions as clamed because the use of Kishida could provide Hirata the ability to designate the range of the instructions being read or fetched in a predetermined instruction format, and therefore, reducing the circuit space of Hirata, and because Hirata already taght the high performance sequential

machines were already known in the art (see col.1, lines 22-25), which was a suggestion for specifying the number of sequential fetch was desirable in order to achieve the high performance sequential processing, and for doing so, provided motivation.

18. As to claim s 14,15, Kishida also included additional fields (see fig.10A).

19. Claim 25, 26,29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata et al. (5,430,851) in view of Cray (3,833,889).

20. A to claim 25, 26, Hirata taught (see fig.2a) :

a) an instruction fetch (IF) memory comprising a sequence of IF instructions (see instruction cache) ;

b) a programmable instruction fetch mechanism comprising means to fetch and execute IF instructions (see instruction fetch units);

c) at least two memory address bus interfaces between the programmable instruction fetch mechanism and at least one processing element (see processing units FP, Integer ALU); and

d) at least two arithmetic/logic (AL) instruction memories (Memories) which interface with the at least two memory address buses (for address buses see how address was given by instruction fetch unit in col.5, lines 65-68, col.6, lines 1-8); at least two AL decode (see decoders) and execute units (see processing units FP, Integer ALU) ; and programmable instruction fetch mechanism operating to fetch IF instructions from said IF memory and executes the fetched IF instructions thereby generating memory

intimation addresses to select processor element (PE) AL instructions singly from one of the AL instruction memories for execution on one of the AL decode and execute units (see each the fetch unit in fig.2a, fig.3, see col.5, lines 10-26).

21. Hirata did not specifically show the set of address registers as claimed. However, disclosed a set of address registers (see fig.3 [103] [105][107] [113]). It would have been obvious to one of ordinary skill in the art to use Cray for including the set of address register as claimed because the sue of Cary could provide Hirata the control capability to access the instructions based on specific address level of operation of the instruction, such as the fetch , and storage, and because Hirata did disclose giving the address for accessing the instructions by the fetch unit (see col.5, lines 65-68), therefore, one of ordinary skill in the art should be able to recognize the use of Cray's address registers into Hirata with modified control parameters (e.g. the address port width) in order to achieved the control adaptability to access the instructions based on specific address registers.

22. As to claim 29, Hirata also included vector and condition of the instructions (see col.26, lines 35-68, see s(t) for vector, see operational directive condition for the condition).

23. Claim 30, 34-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata et al. (5,430,851) in view of Cray (3,833,889) as applied to claim 25, and further in view of Ganapathy et al. (6,557,096).

24. As to claim 30 , neither Hirata nor Cray taught the data type field as claimed. However, Ganapathy taught a data type field (see fig.6). It would have been obvious to use Ganapathy in Hirata because the use of Ganapathy could provide Hirata the ability to specify the data according to the type of data being used, therefor, increasing the ability to accept different type of data in Hirata, and it could be done by reconfiguring the data type field of Ganapathy into Hirata so that the data type field of Ganapathy could be recognized by Hirata to achieve the ability to accept different type of data.

25. As to claims 34-36, although Hirata did not specifically show the 16, 32 and 64 bit immediate fields as claimed. Examiner holds that different length of immediate fields could also be applicable in Hirata because Hirata taught RISC as the background (see col.1, lines 30-35), and the RISC should be able to accept different instruction field widths.

26. Claims 10 ,11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record teaches the combined features of two AL memories, and wherein the identified parallel multiple-issue instructions, control structure instructions, and the sequence of instructions are used to generate IF instructions and their sequencing for programmably selecting instructions to be fetched from said at least two AL memories for execution when parallel multiple-issue AL instructions are indicated (claim 10), and the combined features of identifying single and duplicate AL instructions in a section of code making

up said Program; and removing all but one of the duplicate AL instructions from said at least one AL memory; identifying at what addresses in the program sequence the duplicate AL instructions occur and the address of the single reference AL instruction; and using this identification in generating IF instructions and their sequencing such that whenever a duplicate AL instruction is required, an IF instruction is executed to create the address for the single reference AL instruction stored in said at least one AL memory. whereby a single AL instruction is stored in said at least one AL memory instead of a plurality of duplicate AL instructions for said section of code making up said program (claim 11) .

27. Claim 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record teaches the combined features of types each comprise two additional fields for a loop count and a loop end address; the address of the IF instruction identifying the loop start address which together with said loop end address identities the program loop and the loop count controls the number of iterations of the loop.

28. Claims 17-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record teaches the combined features of the third IF instruction type for parallel multiple-issue instructions; an additional arithmetic/logic (AL) instruction memory (IMemory) comprising a set of

AL instructions; and an additional AL decode and execute unit, said programmable instruction fetch mechanism operating to fetch IF instructions from said IF memory and when executing a third IF instruction type generating at least two IMemory instruction addresses to select AL instructions to be fetched from at least two IMemories for execution on the at least two AL decode and execute units.

29. Claims 23,24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record teaches the combined features of the fifth IF instruction type for parallel multiple-issue instructions; an additional arithmetic/logic instruction memory comprising a set of AL instructions; an additional AL decode and execute unit; and an IMemory and its associated decode and execute units separate from the other memories associated with the AL decode and execute units, said programmable instruction fetch mechanism operating to fetch IF instructions from the IF memory and when executing the fifth IF instruction type generates at least three memory instruction addresses to select instructions to be fetched from at least three memories for execution on the at least two AL decode and execute units and on the separate decode and execute unit.

30. Claims 27,28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record teaches the combined features of the two processor elements controllable as one concatenated processor element with a first type IMemory AL instruction specifying a concatenated

operation, and controllable as two independent processor elements with a second type IMemory AL instruction specifying at least two independent operations.

31. Claim 31 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the combined features of the PE AL instruction format comprises an opcode field, a vector parameter field, a vector address register field, a data memory selection field, and at least one operand field.

32. Claim 32 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the combined features of the PE AL instruction format comprises an opcode field, a vector parameter field, a data type field, a data memory selection field, and at least one vector operand parameter field, at least one address register field, and at least one operand offset field.

33. Claim 33 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the combined features of initiating the vector operation when a PE AL instruction format supporting vector setup operation executes, causing at least one operand address to be

loaded into an address register and starting the vector operation each time a PE AL instruction format supporting vector system is fetched and executed.

34. Claims 37-39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the combined features of the PE AL instructions of a second IMemory AL instruction type are comprised of multiple 32-bit formats (claim 37).

35. Claim 40 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the combined features of at least two clusters of two processor elements each controllable as two processor elements with two different first type IMemory AL instructions, and controllable as four independent processor elements with four different second type IMemory AL instructions.

36. Claim 41 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the combined features of at least two clusters of four processor elements each controllable as two processor elements with two different first type IMemory AL instructions, controllable as four independent processor elements with four different

second type IMemory AL instructions, and controllable as eight independent processor elements with eight different second type IMemory AL instructions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan